Notice of Allowability	Application No.	Applicant(s)	
	10/696,404	CARROLL, DENNIS J.	
	Examiner	Art Unit	
	Giovanna Colan	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment dated 05/21/2007*.

2. ☒ The allowed claim(s) is/are *35-86*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/28/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SANA AL-HASHEMI
PRIMARY EXAMINER

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

2. Per the instant office action, **claims 35 – 86** are considered as allowable subject matter.

The primary reasons for allowance of **claim 35** in the instant application is the combination with the inclusion in these claims of the limitation "designating S memory areas of the memory device as A1, A2, . . . , As; setting an output index P=0 and a field index Q=0; providing a node E having S elements stored therein, said S elements consisting of the S sequences or S pointers respectively pointing to the S sequences" **and together with the limitation** "then generating C child nodes from node E, each child node including all elements in node E having a unique value of field FQ+1, said child nodes denoted as E0, E1, . . . , EC-1 having associated field FQ+1 values of V0, V1, . . . , VC-1, said child nodes E0, E1, . . . , EC-1 being sequenced such that V0<V1< . . . <VC-1; said generating followed by incrementing Q by 1, said incrementing Q followed by iterating from an index I=0 to I=C-1 in steps of 1, wherein iteration I includes setting E=EI followed by executing the program code recursively at the next level of recursion for the node E; else for each element in node E: incrementing P by 1, next storing in AP either U or the element pointing to U, and lastly if the program code at all of said levels of recursion has not been fully executed then resuming execution of said program code at the most previous level of recursion at which the program code was partially but not fully executed else exiting the algorithm".

The primary reasons for allowance of **claims 50** in the instant application is the combination with the inclusion in these claims of the limitation "a computer usable medium having a computer readable program code embodied therein, said computer readable program code comprising an algorithm for sorting S input sequences of binary bits in ascending or descending order of a value associated with each sequence and in a time period denoted as sorting execution time, said S sequences being stored in a memory device of a computer system prior to said sorting, S being at least 2, each sequence of the S sequences comprising K contiguous fields denoted left to right as F1, F2, . . . , Fk with corresponding field widths of W1, W2, . . . , Wk, said algorithm adapted to performed said sorting by executing the steps of: designating S memory areas of the memory device as A1, A2, . . . , As; setting an output index P=0 and a field index Q=0; providing a node E having S elements stored therein, said S elements consisting of the S sequences or S pointers respectively pointing to the S sequences" **and together with the limitation** "then generating C child nodes from node E, each child node including all elements in node E having a unique value of field FQ+1, said child nodes denoted as E0, E1, . . . , EC-1 having associated field FQ+1 values of V0, V1, . . . , VC-1, said child nodes E0, E1, . . . , EC-1 being sequenced such that V0<V1< . . . <VC-1; said generating followed by incrementing Q by 1, said incrementing Q followed by iterating from an index I=0 to I=C-1 in steps of 1, wherein iteration I includes setting E=EI followed by executing the program code recursively at the next level of recursion for the node E; else for each element in node E: incrementing P by 1, next storing in AP either U or the element pointing

to U, and lastly if the program code at all of said levels of recursion has not been fully executed then resuming execution of said program code at the most previous level of recursion at which the program code was partially but not fully executed else exiting the algorithm".

The primary reasons for allowance of **claim 65** in the instant application is the combination with the inclusion in these claims of the limitation "designating S memory areas of the memory device as A1, A2, . . . , As; setting an output index P=0 and a field index Q=0; providing a node E having S elements stored therein, said S elements consisting of the S sequences or S pointers respectively pointing to the S sequences" **and together with the limitation** "then generating C child nodes from node E, each child node including all elements in node E having a unique value of field FQ+1, said child nodes denoted as E0, E1, . . . , EC-1 having associated field FQ+1 values of V0, V1, . . . , VC-1, said child nodes E0, E1, . . . , EC-1 being sequenced such that V0<V1< . . . <VC-1; said generating followed by incrementing Q by 1, said incrementing Q followed by iterating from an index I=0 to I=C-1 in steps of 1, wherein iteration I includes setting E=EI followed by returning to said counter-controlled looping; else for each element in node E: incrementing P by 1, next storing in AP either U or the element pointing to U, and lastly if all the iterations of said outermost loop have not been executed then returning to said counter-controlled looping else exiting from said algorithm".

The primary reasons for allowance of **claim 76** in the instant application is the combination with the inclusion in these claims of the limitation "a computer usable medium having a computer readable program code embodied therein, said computer readable program code comprising an algorithm for sorting S input sequences of binary bits in ascending or descending order of a value associated with each sequence and in a time period denoted as sorting execution time, said S sequences being stored in a memory device of a computer system prior to said sorting, S being at least 2, each sequence of the S sequences comprising K contiguous fields denoted left to right as F1, F2, . . . , Fk with corresponding field widths of W1, W2, . . . , Wk, said algorithm adapted to performed said sorting by executing the steps of: designating S memory areas of the memory device as A1, A2, . . . , As; setting an output index P=0 and a field index Q=0; providing a node E having S elements stored therein, said S elements consisting of the S sequences or S pointers respectively pointing to the S sequences" **and together with the limitation** "then generating C child nodes from node E, each child node including all elements in node E having a unique value of field FQ+1, said child nodes denoted as E0, E1, . . . , EC-1 having associated field FQ+1 values of V0, V1, . . . , VC-1, said child nodes E0, E1, . . . , EC-1 being sequenced such that V0<V1< . . . <VC-1; said generating followed by incrementing Q by 1, said incrementing Q followed by iterating from an index I=0 to I=C-1 in steps of 1, wherein iteration I includes setting E=EI followed by returning to said counter-controlled looping; else for each element in node E: incrementing P by 1, next storing in AP either U or the element pointing to U, and lastly if all the iterations of

said outermost loop have not been executed then returning to said counter-controlled looping else exiting from said algorithm ".

The prior art of record neither anticipates nor renders obvious the above-recited combination.

Dependent **claims 36 – 49, 51 – 64, 66 – 75, and 77 – 86** are allowable at least for the reasons recited above as including all of the limitations of the allowable independent base claims upon which they depend.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issues fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Points Of Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Giovanna Colan whose telephone number is (571) 272-2752. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Giovanna Colan
Examiner
Art Unit 2162
July 26, 2007

SANA AL-HASHEMI
PRIMARY EXAMINER